IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	09/301,438	Confirmation No.:	5559
First Named Inventor:	Wolf, Christopher K.	Filing Date:	28 April 1999
Group Art Unit:	2665	Examiner:	Nguyen, S.
Atty. Docket No.:	NS-3799 US		
Title:	System and Method for Decoding Audio/Video Data such as DVD or/and DVB Data		
Assignee(s):	National Semiconductor Corp.		

DECLARATION OF ALIN THEODOR IACOB

I, Alin Theodor Iacob, declare as follows:

1. I am an electrical engineer employed at National Semiconductor Corporation ("NSC"), the assignee of the above patent application. I have worked as an electrical engineer for seventeen years, including the last fourteen years at NSC.

2. I have a Master of Science from Polytechnical Institute of Bucharest in electrical engineering.

3. I am the sole inventor on U.S. patent application 09/899,406, now U.S. Patent 6,531,825 B1, and an inventor on other pending U.S. patent applications.

4. A first-in-first-out ("FIFO") buffer is an electronic data storage device in which data is removed from (read out from) the device in the same order that the data is provided to (written into) the device. A FIFO buffer has a single input port and a single output port, both of which are normally of the same bit width. Similar to how a shift register operates, the data in a FIFO buffer automatically passes from the input port to the output port. As such, a FIFO buffer does not have multiple addressable locations for storing data.

5. I have reviewed the specification and drawings of the above U.S. patent application, including the specification as filed..

6. The specification, as filed, states on page 7 that "SD 26 demultiplexes and depacketizes the data stream, storing the demultiplexed compressed audio and video data in data buffer 48 which is typically a First-In-First-Out (FIFO) buffer" and that "SD 26 has

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access to 32 different addressable locations in FIFO 48". The specification, as filed, repeats the disclosure that buffer 48 has multiple addressable locations with the statement on page 23 that "In one embodiment, the system memory includes thirty-two separate buffers (e.g., buffer 48 includes thirty-two separate sub-buffers): one buffer each for MPEG video, audio, sub-picture, teletext, and various other data and control streams".

7. The specification, as filed, states on page 10 that "In other words, for each data pack 200, SD 26 generates a tag containing information about both the decode time stamp as well as the address of the stored data in FIFO 48". The specification, as filed, later states on page 10 that "Therefore, if a faster data consumption rate is necessary, CPU 54 skips over the next frame of data in FIFO 48 and thus issues a TDP pointing to the address of the succeeding data frame in FIFO 48".

8. Inasmuch as (a) buffer 48 has 32 different data-storage locations and (b) a FIFO buffer does not have multiple addressable data-storage locations, buffer 48 is not a FIFO in hardware or a FIFO buffer in hardware despite being described as a "FIFO" at various places in the specification, as filed. On information and belief, the fact that buffer 48 is not a FIFO in hardware or a FIFO buffer in hardware would also generally be recognized by other persons skilled in the semiconductor memory art.

9. More particularly, buffer 48 is part of a random-access memory ("RAM"), such as a static RAM or a dynamic RAM, having multiple addressable storage locations. This is clear from page 25 of the specification, as filed, where it is stated that "In particular, the tags contain addresses in the system memory (e.g., in a RAM, DRAM, or SRAM that includes buffer 48 of Fig. 1) where data associated with certain events in the input stream can be found".

10. Certain of the sub-buffers of buffer 48 operate in a FIFO manner in that the information first placed in each such sub-buffer is the information first to be removed from that sub-buffer. This FIFO-like operation is achieved by appropriately controlling the placement of information in, and the removal of information from, each such sub-buffer using, for example, a memory management unit as described on pages 22 - 25 of the specification, as filed. However, the information placed in any of the 32 sub-buffers of buffer 48 is not limited to being the first information removed from buffer 48. Accordingly, buffer 48 is not a FIFO in hardware or a FIFO buffer in hardware and, on information and belief, would not generally be recognized as a FIFO in hardware or a FIFO buffer in hardware by persons skilled in the semiconductor memory art.

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11. Buffer 48 can be accurately described simply as a buffer.

I further declare that all statements made herein of my own knowledge are true, that all statements made herein on information and belief are believed to be true, that all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the U.S. Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

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6/30/2005
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